AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (cancelled)

2. (currently amended) A FET as in claim [[1]] 48, wherein said fin is a semiconductor fin selected from a group of materials consisting of silicon, germanium and silicon-germanium.

3. (original) A FET as in claim 2, wherein said fin is a silicon fin.

4. (cancelled)

5. (currently amended) A FET as in claim [[1]] 48, wherein said back bias gate dielectric is thicker than said gate dielectric.

6. (currently amended) A FET as in claim [[1]] 48, wherein each of said back bias gate dielectric and said gate dielectric is selected from a group of materials consisting of an oxide, an oxynitride and a high K dielectric.

7. (currently amended) A FET as in claim [[1]] 48, wherein said gate and said back bias gate are a conductive material selected from a group of materials consisting of a metal, doped silicon, doped germanium, doped silicon germanium and a metal silicide.

8. (original) A FET as in claim 3, wherein said dielectric surface is an oxide layer.

9. (original) A FET as in claim 8, wherein said oxide layer is a buried oxide layer.

10. (original) A FET as in claim 8, wherein said oxide layer is disposed on a nitride layer.

11. (original) A FET as in claim 3, further comprising a dielectric pillar above said silicon fin.

12. (original) A FET as in claim 11, wherein said dielectric pillar is a nitride pillar.

13. (original) A FET as in claim 12, wherein said nitride pillar forms a cap between said device gate and said back bias gate.

14. (cancelled)

15. (cancelled)

16. (currently amended) An IC as in claim [[14]] 49, wherein each of said back bias gate dielectric and said gate dielectric is selected from a group of materials consisting of an oxide, an oxynitride and a high K dielectric.

17. (cancelled)

18. (currently amended) An IC as in claim [[14]] 49, wherein said gate and said back bias gate are a conductive material selected from a group of materials consisting of a metal, doped silicon, doped germanium, doped silicon germanium and a metal silicide.

19. (currently amended) An IC as in claim [[14]] 49, wherein said dielectric surface is an oxide layer.

20. (original) An IC as in claim 19, wherein said oxide layer is a buried oxide layer.

21. (original) An IC as in claim 19, wherein said oxide layer is disposed on a nitride layer.

22. (currently amended) An IC as in claim [[14]] 49, each said FET further comprising a dielectric pillar above said semiconductor fin.

23. (original) An IC as in claim 22, wherein said dielectric pillar is a nitride pillar.

24. (original) An IC as in claim 23, wherein said nitride pillar forms a cap between said device gate and said back bias gate.

25. (original) An IC as in claim 22, wherein said semiconductor is silicon.

26 – 47 (cancelled)

48. (new) A field effect transistor (FET) comprising:

a fin formed on a dielectric surface;

a device gate along one side of said fin;

a back bias gate along an opposite side of said fin;

device gate dielectric along one first side between said device gate and said fin; and

back bias gate dielectric along said opposite side between said back bias gate and said fin, wherein said back bias gate dielectric differs from said device gate dielectric in material, wherein one of said device gate dielectric and said back bias gate dielectric are a layered dielectric comprising at least 2 dielectric material layers.

49. (new) An integrated circuit (IC) on a semiconductor on insulator (SOI) chip, said IC including a plurality of field effect transistors (FETs) disposed on an insulating layer, each of said FETs comprising:

a semiconductor fin formed on an insulating layer;

device gate dielectric along a first side of said semiconductor fin;

a device gate along said device gate dielectric;

back bias gate dielectric along an opposite of said semiconductor fin; and

a back bias gate along said back bias gate dielectric, wherein said back bias gate dielectric is five times (5X) thicker than said gate dielectric.

50. (new) An integrated circuit (IC) on a semiconductor on insulator (SOI) chip, said IC including a plurality of field effect transistors (FETs) disposed on an insulating layer, each of said FETs comprising:

a semiconductor fin formed on an insulating layer;

device gate dielectric along a first side of said semiconductor fin;

a device gate along said device gate dielectric;

back bias gate dielectric along an opposite of said semiconductor fin;

a back bias gate along said back bias gate dielectric, wherein said back bias gate dielectric differs from said device gate dielectric of material, wherein one of said device gate dielectric and said back bias gate dielectric are a layered dielectric comprising at least 2 dielectric material layers.

51. (new) An IC as in claim 50, wherein said gate and said back bias gate are a conductive material selected from a group of materials consisting of a metal, doped silicon, doped germanium, doped silicon germanium and a metal silicide.

52. (new) An IC as in claim 50, wherein said dielectric surface is an oxide layer.

53. (new) An IC as in claim 52, wherein said oxide layer is a buried oxide layer.

54. (new) An IC as in claim 52, wherein said oxide layer is disposed on a nitride layer.

55. (new) An IC as in claim 50, each said FET further comprising a dielectric pillar above said semiconductor fin.

56. (new) An IC as in claim 55, wherein said dielectric pillar is a nitride pillar.

57. (new) An IC as in claim 56, wherein said nitride pillar forms a cap between said device gate and said back bias gate.

58. (new) An IC as in claim 55, wherein said semiconductor is silicon.